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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,760	07/21/2003	Rajiv V. Joshi	909A.0128.U1(US)	1720

29683 7590 11/08/2004

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EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,760	JOSHI ET AL.	
	Examiner	Art Unit	
	Thinh T Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Applicants' election of claims 1-8 for prosecution of the present application in the communication with the Office on 10/12/2004 is acknowledged.

Specification

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claim Objections

3. Claim 8 is objected to for the following informalities:

In claim 8 line 1 " field effect **transmitter** " should be – field effect **transistor** – Correction or clarification is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an

application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1-2,6-7,8 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugiyama et al. (U.S. Patent 6,774,390) or Dakshina-Murthy et al. or Clark et al (US patent 6,635,909).

REGARDING CLAIM 1-2

Sugiyama et al. (in the abstract, in fig 2, column 6 lines 63-67, column 7 lines 1-10) disclose a channel for electrically connecting a source and a drain of a field effect transistor (FET) comprising: a channel core (fig 2, reference 30) coupled to a substrate and defining a top surface spaced from the substrate and opposed sidewall surfaces between the substrate and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure; a channel envelope (fig 2 reference 40) in contact with the opposed sidewall surfaces and the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; and a gate oxide disposed about a surface of the channel envelope that is opposite the channel core with the channel further comprising a gate(fig 2 reference 80) coupled through the gate oxide (fig 2 reference 70) to at least two surfaces defined by the channel envelope.

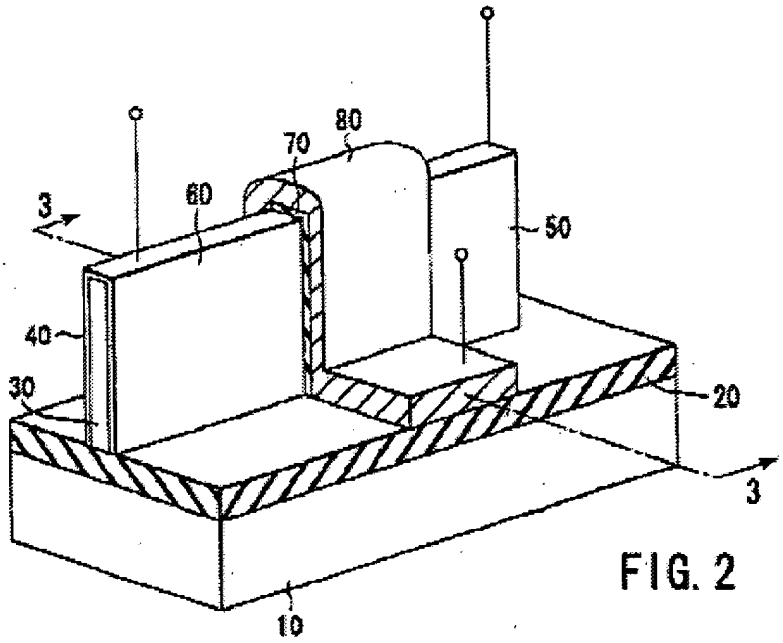

FIG. 2

Similarly Dakshina-Murthy et al. (the abstract, fig 4A) and Clark et al (fig 31, the abstract, column 3 line 45-56) disclose the same inventions.

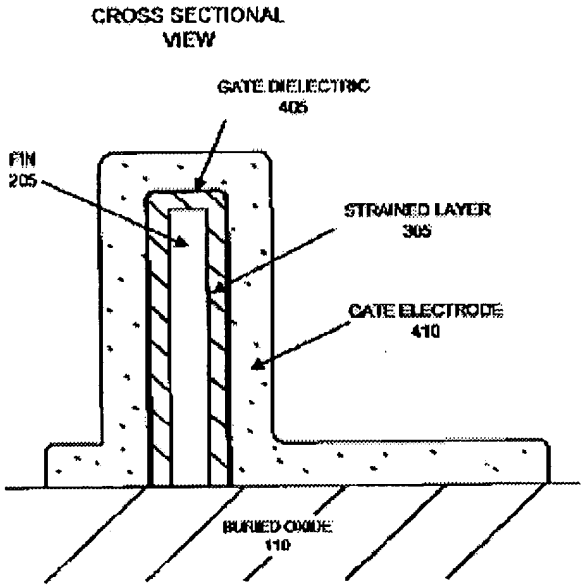

FIG. 4A

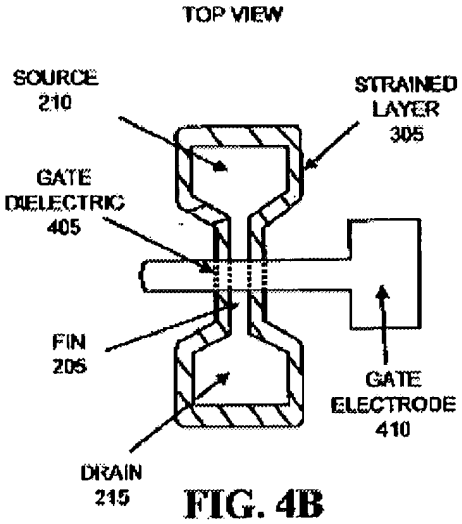

FIG. 4B

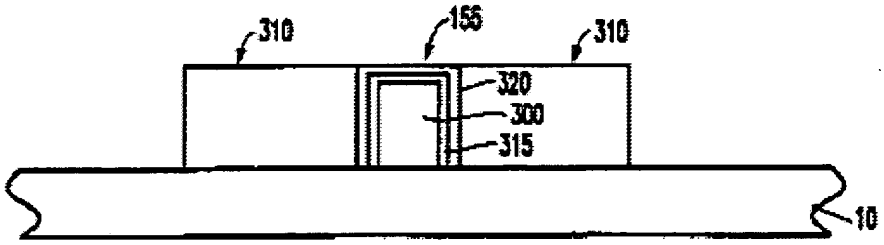

FIG.31

REGARDING CLAIM 6-7

Sugiyama et al. (in the abstract, in fig 2, column 6 lines 63-67, column 7 lines 1-10) disclose a channel for electrically connecting a source and a drain of a field effect

transistor (FET) wherein the second semiconductor material substantially covers the two sidewall surfaces and the top surface and wherein one of the first and second semiconductor materials comprises silicon and germanium.

Similarly Dakshina-Murthy et al. (the abstract, fig 4A, column 3 lines 19-36) and Clark et al (fig 31, the abstract, column 3 line 45-56) disclose the same inventions.

REGARDING CLAIM 8

Sugiyama et al. (in the abstract, in fig 2, column 6 lines 63-67, column 7 lines 1-10) disclose a channel for a field effect transistor , the improvement comprising: a channel core defining at least a top and at least one adjoining side surface, and a channel envelope in contact with the top surface and the at least one side surface, and a gate oxide disposed on at least two surfaces of the channel envelope, said surfaces of the channel envelope being opposed to the top surface and the at least one side surface, wherein the channel core comprises a first semiconductor material and the channel envelope comprises a second semiconductor material, and at least one of the first and second semiconductor materials exhibits one of a stretched and a compressed lattice structure.

Similarly Dakshina-Murthy et al. (the abstract, fig 4A, column 3 lines 19-36) and Clark et al (fig 31, the abstract, column 3 line 45-56) disclose the same inventions.

7. Claim 3 is rejected under 35 U.S.C. 102(e) as being anticipated by Sugiyama et al. (U.S. Patent 6,774,390)

REGARDING CLAIM 3

Sugiyama et al. (in the abstract, in fig 7, in column 9 line 30-43) disclose the width of the channel (Sugiyama called it the board) being from 10 to 50 nanometer and the height being from the range of 50 nanometer to 1 micrometer therefore fully anticipated the limitation :

(height) Hc ≥ (width) 3 Wc as recited in claim 3

Claim Rejections - 35 USC § 103

8. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. (U.S. Patent 6,774,390) in view of further remark.

REGARDING CLAIM 5

Sugiyama et al. disclose all the invention except for the condition that the width of the channel is selected to maximize one of stretching and of compressing the lattice structure of one of the first and the second semiconductor material.

This feature, however, is considered obvious since it has been held that when all the general conditions of a claim is disclosed in prior art; discovering the optimum value or workable range is within the routine skills or a person with ordinary skills in the art.

A person skilled in the art at the time the invention was made would have been able to find out these values using his regular design skill without any special teachings with the motivation of improving the semiconductor device.

10. Claim 4 is rejected under 35 USC 103(a) as being unpatentable over Sugiyama et al. (U.S. Patent 6,774,390) in view of further remark.

REGARDING CLAIM 4

Sugiyama et al. (in the abstract, in fig 2, column 6 lines 63-67, column 7 lines 1-10) disclose all the invention including a channel is a component of an FET missing in Sugiyama et al. is the disclosure that the FET is a component of a SRAM, and at least one of the sidewall surfaces defines a height hc that is selected to increase stability of the SRAM. a channel of the SRAM.

Sugiyama et al., however , disclose (column 4 lines 54-55) that their devices are CMISFET (CMOS technology) and the use of CMISFET in SRAM (static ram) is old and well known in the art as shown in Krivokapic et al. (US patent 6,765,303).

It would have been obvious to one of ordinary skill in the art the time the invention was made to use the teachings by Sugiyama et al. and his ordinary design skill in order to came up with the invention of claim 4.

The rationale is the same as in the rejection of claim 5 except this time the width of the channel is involved.

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

CONCLUSION

13. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Yu (US patent 6,300,182) discloses a Field effect transistor having dual gates with asymmetrical doping for reduced threshold voltage

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen TTN

Art Unit 2818

David Nelms
Supervisory Patent Examiner
Technology Center 2800